CLAIMS

1. A method of forming a trench isolation structure comprising the steps of:

supplying a microelectronic substrate;

forming a trench in the microelectronic substrate;

depositing a field oxide in the trench, the field oxide projecting above the substrate to a height that is small enough to prevent the formation of spacers about the field oxide.

2. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

forming a trench in the microelectronic substrate;

depositing a field oxide in the trench extending from the trench to a height which is less than half of a height of a gate structure to be formed on the substrate;

forming the gate structure on the substrate; and

forming a spacer adjacent the gate structure.

3. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

depositing a field oxide isolation pad extending from a recess in the substrate to a field oxide isolation pad height;

forming a gate structure on the substrate having a height which is at least twice the height of the field oxide isolation pad height; and

forming a spacer adjacent the gate structure.

4. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

forming a trench in the microelectronic substrate;

depositing a field oxide isolation pad extending from the trench by height which is less than half of a height of a component to be formed on the field oxide isolation pad;

forming the component on the field oxide isolation pad; and

forming a spacer adjacent the component.

5. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

depositing a field oxide isolation pad extending from a recess in the substrate to a field oxide isolation pad height;

forming a component on the field isolation pad having a height which is at least twice the height of the field oxide isolation pad height; and

forming a spacer adjacent the component.

6. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

growing a gate oxide layer on the microelectonic substrate;

depositing a first gate layer on the gate oxide layer;

forming a trench, the trench extending though the first gate layer, the gate oxide layer and into the substrate;

filing the trench with a field oxide;

planarizing the field oxide;

recessing the field oxide;

depositing a second gate layer over the recessed field oxide and the first gate layer;

forming a silicide layer over the second gate layer;

forming at least one gate structure in the silicide layer, the first and the second gate layers and the gate oxide layer; and

forming a spacer adjacent the gate structure.

7. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is below an upper surface of the first gate layer.

8. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is above an upper surface of the substrate.

9. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is between an upper level of the first gate layer and an upper level of the substrate.

10. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a depth that is below an upper level of the first gate layer and that is at least even with an upper level of the substrate.

11. The method of claim 6 wherein the step of recessing the field oxide includes the step of

recessing the field oxide to a level which extends beyond an upper level of the substrate by a height which is less than or equal to approximately one half of a height of the gate structure.

12. The method of claim 11, further comprising the step of

depositing a stop layer on the first gate layer before etching the trench.

13. The method of claim 12, wherein the step of forming a trench includes the step of

etching through the stop layer, the first gate layer, the gate oxide layer; and etching into the substrate.

14. The method of claim 13, further comprising the step of

removing the stop layer after planerizing the field oxide.

15. The method of claim 6 wherein the step of depositing a first gate layer includes the step of

depositing a layer of polysilicon on the gate oxide layer.

16. The method of claim 6 wherein the step of depositing a second gate layer includes the step of

depositing a layer of polysilicon on the recessed field oxide and the first gate layer.

17. The method of claim 6 wherein the step of forming a silicide layer includes the step of

depositing a layer of tungsten silicide on the second gate layer by chemical vapor disposition.

18. The method of claim 6, wherein the step of forming the silicide layer includes the step of:

depositing a conductor by chemical vapor disposition on at least one of the first and the second gate layers; and

reacting the metal with the at least one of the first and the second gate layers to form a silicide.

19. A method of forming a trench isolation structure on a microelectronic substrate, the method comprising the steps of:

growing a gate oxide layer on the microelectronic substrate;

depositing a polysilicon gate layer on the gate oxide layer;

depositing a nitride stop layer on the polysilicon gate layer;

etching a trench though the nitride stop layer, the polysilicon gate layer, and the gate oxide layer, the trench extending into the substrate;

filing the trench with a field oxide;

planerizing the field oxide through chemical-mechanical planarization;

removing the nitride stop layer;

recessing the planerized field oxide to a depth that is below an upper level of the polysilicon gate layer and that is at least even with an upper level of the substrate;

depositing a polysilicon adherence layer superjacent the polysilicon gate layer and the recessed field oxide;

depositing a tungsten silicide layer over the polysilicon adherence layer;

forming at least one gate structure in the tungsten silicide layer, the polysilicon adhesion layer and the polysilicon gate layer; and

forming at least one spacer adjacent the gate structure.

20. The method of claim 19 further comprising the step of:

forming an oxide on the tungsten silicide layer before performing the forming at least one gate structure step.

21. The method of claim 19, wherein the step of forming the gate structure, comprises the steps of:

patterning the tungsten silicide layer; and

etching the tungsten silicide layer and the polysilicon gate layer.

22. A microelectronic device, comprising:

a microelectronic substrate;

a gate oxide layer formed on the substrate;

a polysilicon gate layer formed on the gate oxide layer;

a trench defined through the polysilicon gate layer, the gate oxide layer and extending into the substrate; and

a field oxide in the trench, the field oxide having a field oxide level between the level of an upper surface of the substrate and the level of an upper surface of the polysilicon gate layer.

23. A microelectronic device, comprising:

a microelectronic substrate;

a gate oxide layer formed on the substrate;

a polysilicon gate layer formed on the gate oxide layer;

a trench defined through the polysilicon gate layer, the gate oxide layer and extending into the substrate;

a field oxide in the trench, the field oxide having a field oxide level between the level of an upper surface of the gate oxide and the level of an upper surface of the polysilicon gate layer;

a ploysilicon adhesion layer formed over the polysilicon gate layer and the upper surface of the field oxide.

24. The microelectronic device of claim 23, further comprising

a silicide layer formed over the polysilicon adhesion layer.

25. The microelectronic device of claim 23, further comprising

a tungsten silicide layer formed over the polysilicon adhesion layer.

26. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide extending from the trench, beyond the surface of the substrate;

a component formed on the field oxide, the component extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

27. The microelectronic device of claim 26, further comprising an oxide spacer adjacent the component.

28. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a field oxide in the trench, the field oxide extending from the trench, beyond the surface of the substrate;

a gate structure formed on the substrate, the gate structure extending from the field oxide by a height at least equal to approximately two times a height that the field oxide extends from the trench beyond the surface of the substrate.

29. The microelectronic device of claim 28, further comprising an oxide spacer adjacent the gate structure.

30. A microelectronic device, comprising:

a microelectronic substrate having a recess formed in a surface thereof; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate, by a height which is less than approximately one half of a height of a component formed on the field oxide.

31. The microelectronic device of claim 30, further comprising an oxide spacer adjacent the component.

32. A microelectronic device, comprising:

a microelectronic substrate having a trench formed in a surface thereof;

a gate structure formed on the substrate; and

a field oxide deposited in the trench, the field oxide extending from the trench beyond the surface of the substrate, by a height which is less than approximately one half of a height of the gate structure formed on the substrate.

33. The microelectronic device of claim 32, further comprising an oxide spacer adjacent the gate structure.

34. A microelectronic device, comprising:

a microelectronic substrate having a trench formed therein,

a field oxide within the trench and projecting therefrom by a height which is small enough to prevent the formation of spacers adjacent the field oxide pad.